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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Kabune et al.	Atty. Dkt.: 01-129
Serial No.: 09/824,709	Art Unit: 2116
Filed: 4/4/2001	Examiner: Paul B. YANCHUS III
Title: ELECTRONIC CONTROL APPARATUS HAVING A PLURALITY OF POWER SOURCE CIRCUITS	

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Date: 19 July 2005

BRIEF ON APPEAL UNDER 37 C.F.R. § 1.192

Sir:

Appellants hereby submit one copy of their Brief on Appeal under 37 C.F.R. § 1.192.

1. REAL PARTY IN INTEREST

The real party in interest is DENSO Corporation, the assignee by virtue of an assignment recorded at Reel/Frame 011665/0097.

2. RELATED APPEALS AND INTERFERENCES

There is no known related appeal or interference that will directly affect, that will be directly affected by, or that will have a bearing on the Board's decision on this appeal.

3. STATUS OF CLAIMS

Claims 1 – 3 and 6 – 7 are pending in the present application and are included in the attached Appendix A. Claims 1 – 3 and 6 – 7 have been rejected and are now being appealed. Claims 4 – 5 were canceled in the Amendment filed on September 9, 2004.

4. STATUS OF AMENDMENTS

All amendments submitted by Appellants have been entered.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The subject matter of independent claim 1 is discussed with reference to Figs. 2, 3, 7 and 8. In the illustrated embodiment of an electronic control apparatus, there are a plurality of power source circuits (82a, 82b, Figs. 3, 7; page 15, line 20 – page 17, line 23) providing a plurality of power sources of a plurality of different voltages, and a microcomputer (60, Fig. 2). Any one of the plurality of power sources is used as a power source of the microcomputer. The microcomputer is reset immediately when it is detected (comparators 501, 505, Fig. 8) that any one of the plurality of power sources is not set to a voltage in respective specified ranges (VBG1, VBG2, Fig. 5) by checking whether the plurality of power sources are respectively set to the voltages in the specified ranges (e.g., page 12, line 5 – page 13, line 3).

The subject matter of independent claim 6 is discussed with reference to Figs. 2, 3, 7 and 8. In the illustrated embodiment of an electronic control apparatus, there are a plurality of power source circuits (82a, 82b, Figs. 3, 7; page 15, line 20 – page 17, line 23) providing a plurality of power sources of a plurality of different voltages; a microcomputer (60, Fig. 2); and detecting

means (comparators 501, 505, Fig. 8 ; page 21, line 9 – page 24, line 16) for detecting that the plurality of the power sources are set to respective specified voltages (VBG1, VBG2, Fig. 5) when the plurality of power sources are driven. Any one of the plurality of power sources is used as the power source of the microcomputer. The microcomputer is reset (506-511, Fig. 8) immediately when it is detected that any one of the power sources reaches the respective specified voltages (e.g., page 12, line 5 – page 13, line 3).

The subject matter of independent claim 7 is discussed with reference to Figs. 2, 3, 7 and 8. In the illustrated embodiment of an electronic control apparatus there are first and second power source circuits (82a, 82b, Figs. 3, 7; page 15, line 20 – page 17, line 23) providing first and second power sources with first and second voltages different from one another, respectively. A microcomputer (60, Fig. 2) is connected to the first and second power source circuits and operable with the first and second voltages. A first abnormality detection circuit (comparator 501, Fig. 8; page 21, line 9 – page 24, line 16) detects an abnormal value of the first voltage and an abnormal value of a first current in the first power source circuit, the abnormal levels of the first voltage and the first current being outside predetermined first voltage and current ranges (VBG1, VBG2, Fig. 5), respectively. A second abnormality detection circuit (comparator 505, Fig. 8; page 21,line 9 – page 24, line 16) detects an abnormal value of the second voltage and an abnormal value of a second current in the second power source circuit, the abnormal values of the second voltage and the second current being outside predetermined second voltage and current ranges, respectively. A reset control circuit (506-511, Fig. 8) immediately resets the microcomputer in response to an abnormality signal generated by either of the first and the second abnormality detection circuits (e.g., page 12, line 5 – page 13, line 3; page 23, line 7 – page 25, line 2).

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 2 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki in view of Curiger.

Claims 3 and 7 stand rejected under 35 USC 103(a) as being unpatentable over Yamasaki in view of Curiger, further in view of Carter.

7. ARGUMENT

A. Whether claims 1, 2 and 6 are unpatentable under 35 USC 103(a) U.S. over Patent No. 5,339,446, Yamasaki et al. in view of U.S. Patent No. 6,330,668, Curiger et al.

Claim 1 recites, in combination, that "the microcomputer is reset immediately when it is detected that any one of the plurality of power sources is not set to a voltage in respective specified ranges ..."

The configuration as recited in claim 1 provides for immediately resetting the microcomputer when one of the power sources is outside the operating voltage level. Thereby, uncontrolled operation of the microcomputer and unstable I/O output can be prevented. (Specification page 25 lines 8 – 17.)

In the Final Rejection dated April 14, 2003 (hereinafter "the Final Rejection"), the Examiner rejected claims 1, 2 and 6 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,339,446, Yamasaki et al. ("Yamasaki") in view of U.S. Patent No. 6,330,668, Curiger et al. ("Curiger"). Specifically, the Examiner stated that Yamasaki teaches the plurality of power source circuits as recited, the microcomputer, and the detection of whether any one of the power sources is not in a specified voltage range. The examiner acknowledges that Yamasaki teaches stopping the power supply when the voltage of one of the power sources is

outside a normal range, but does not teach resetting the microcomputer when the voltage abnormality is detected. Curiger is cited as teaching the resetting of a microcontroller immediately after it is detected that voltage supply drops below a predetermined voltage.

1. There is no *prima facie* case of obviousness because there is no motivation to combine the references.

To establish a *prima facie* case of obviousness with respect to a claimed invention, all the claim limitations must be taught or suggested by the prior art reference (or references when combined). *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. There must also be a reasonable expectation of success. Furthermore, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991).

The examiner bears the burden of establishing this *prima facie* case. In re Deuel, 34 U.S.P.Q.2d 1210, 1214 (Fed. Cir. 1995). The applicant for patent may then attack the *prima facie* case as improperly made out, or present objective evidence tending to support a conclusion of nonobviousness. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992).

Where, as here, the Examiner fails to establish a *prima facie* case of obviousness, Appellant has no burden to rebut the rejection of obviousness with evidence. In re Rijckaert, 28 U.S.P.Q.2d 1955, 1957 (Fed. Cir. 1993). If the examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more Appellant is entitled to grant of patent. In re Oetiker, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992).

With regard to independent claims 1 and 6, the Final Office Action contends that Yamasaki suggests or teaches the invention as claimed, with the exception of resetting the microcomputer immediately upon certain conditions (Final Office Action page 3).

To the contrary, Appellant provides herein non-exhaustive examples of Yamasaki's deficiencies. Yamasaki does not teach or suggest, for example, the "the microcomputer is reset" (independent claim 1). As merely one particular example of another of Yamasaki's failings, Yamasaki further fails to disclose that the resetting is performed "immediately."

Appellants respectfully assert that Yamasaki does not disclose "immediately" resetting the microcomputer or even "immediately" stopping the power supply. Yamasaki discloses a computer system power supply that is stopped when a voltage abnormality is detected (col. 3, lines 17 – 25). However, the power supply is stopped only after a delay to ensure that various save operations of the computer are completed before system power off is completed. (E.g., col. 6, lines 3 – 42.)

Moreover, although Yamasaki discloses stopping the power supply, Yamasaki fails to disclose "resetting" the microcomputer, and does not provide any discussion thereof. To the contrary, Yamasaki is concerned with an orderly power off sequence.

Recognizing that Yamasaki fails to teach and/or suggest the invention as claimed, Curiger is cited to remedy the deficiencies. For reasons including, for example, that Yamasaki teaches a power off sequence with delay before powering off the microcomputer, Curiger fails to remedy such deficiencies.

Curiger describes an integrated circuit that is reset when the voltage goes below a predetermined voltage (col. 7, lines 27 – 30) and when the temperature falls outside of a predetermined temperature window (col. 8, lines 8 – 10) so that the circuitry is not stressed by

operating at clock speeds, temperatures or voltages that are greater than those for which it is designed. Such stress can cause the circuitry to introduce undesirable errors into calculations (col. 1, lines 54 – 57). Curiger does not explicitly discuss immediately resetting a microcomputer.

There is no suggestion or motivation to combine the Yamasaki and Curiger in the manner proposed in the office action. "There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination." In re Oetiker, 977 F.2d 1443, 24 USPQ.2d 1443 (Fed. Cir. 1992). Moreover, to establish a *prima facie* case of obviousness, "it is necessary for the examiner to present evidence, preferably in the form of some teaching, suggestion, incentive, or inference in the applied prior art, or in the form of generally available knowledge, that one having ordinary skill in the art would have been led to combine the relevant teachings of the applied references in the proposed manner to arrive at the claimed invention." In re Levengood, 28 USPQ.2d 1300, 1301 (Bd. Pat. App. 1993).

"Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed." In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ.2d 1313, 1317 (Fed. Cir. 2000). See also, Crown Operations Int'l Ltd. v. Solutia Inc., 289 F.3d 1367, 1376, 62 USPQ.2d 1917 (Fed Cir. 2002) ("there must be a teaching or suggestion within the prior art, within the nature of the problem to be solved, ... to look to particular elements, and to combine them as combined by the inventor".)

The motivation provided for combining the references is the statement in page 3 of the Final Office Action that the combination of Yamasaki and Curiger would be made because

Curiger allegedly teaches "resetting a microcomputer immediately after it is detected that a power source output is not in the proper voltage range ensures that the microcomputer will not perform incorrect calculations." The final office action relies on Curiger, col. 1 lines 64 – 67 and col. 2 lines 12 – 17, in the summary of the invention which states:

> In doing so, the integrated circuit, and more particularly, the microcontroller is prevented from providing or performing an incorrect calculation result under certain conditions. ...
>
> ... Furthermore, a voltage sensing circuit can be incorporated into the present embodiment and sense when the voltage provided to the silicon circuit is above or below a predetermined range and thereby stop the silicon circuitry from being stressed to produce an invalid or incorrect calculation result.
>
> Curiger, col. 1 lines 64 – 67 and col. 2 lines 12 – 17.

As noted by the examiner, Yamasaki, col. 3, lines 17 – 25 discloses a computer system power supply that is stopped when a voltage abnormality is detected. However, the power supply is stopped only after a delay to ensure that various save operations of the computer are completed before system power off is completed. (E.g., col. 6, lines 3 – 42).

The Advisory Action states that "one would be motivated to apply the teachings of Curiger to the Yamasaki system to reset the microcomputer immediately after an abnormal voltage is detected to ensure that information is not inadvertently overwritten or lost during a system shutdown procedure due to improper functionality of the system due to abnormal supply voltages." The examiner's proposed motivation is misleading – immediately resetting Yamasaki's system would result in overwriting information, and may well prevent completion of any remaining processing during a system shutdown procedure.

Curiger describes an integrated circuit that is reset when the circuit is operating under stress conditions that can cause the circuitry to introduce undesirable errors into calculations (col. 1, lines 54 – 57). One cannot glean from Yamasaki a motivation to combine its save operation and delayed stop power supply with Curiger's stress-prevention circuitry. Nor can one glean

from Curiger's stress-prevention circuitry a motivation to be included as part of a delayed stop such as provided by Yamasaki.

In determining whether a suggestion can be fairly gleaned from the prior art, one must consider the full field of the invention, "including that which might lead away from the claimed invention." In re Dow Chemical, 837 F.2d 469, 473, 5 USPQ.2d 1529, 1531 (Fed. Cir. 1988). Yamasaki teaches a power off sequence that performs a save operation to save contents of registers, etc., for restarting an interrupted job. Curiger assumes, to the contrary, that the contents of the registers, etc. should be discarded. Hence it appears that the references implicitly and explicitly lead away from the invention as claimed.

Moreover, assuming *arguendo* that it may have been possible to combine both, that in itself provides no motivation to combine the references as proposed by the Examiner. To the contrary, where proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). In this case, modifying Yamasaki as proposed to include an immediate reset would render Yamasaki unsatisfactory for its intended purpose of providing a power down sequence.

Claims 2 – 3 depend from independent claim 1, and are non-obvious for at least the foregoing reasons.

2. The Proposed Combination fails to teach or suggest the invention as a whole.

Assuming *arguendo* the suggested motivation, the proposed combination of references still fails to teach or suggest the invention as claimed. For example, the combination of Yamasaki and Curiger still fails to provide an immediate reset upon detecting that one of the power sources is outside a voltage range.

The claimed subject matter "as a whole" must be considered in determining obviousness. E.g., Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc., 796 F.2d 443, 449, 230 USPQ 416, 420 (Fed. Cir. 1986). Here, the proposed combination fails to teach at least one feature taken in combination with the remainder of features of the claimed invention.

Assuming *arguendo* a motivation to combine the two references, the proposed modification would appear to change the principle of operation of either Yamasaki or Curiger, or both. Yamasaki claims to be a power supply for use in a computer system which performs a power off sequence. The Office Action argues that Curiger teaches an immediate reset of the microcomputer (Final Office Action ¶ X). Assuming *arguendo* that Curiger provides the teaching as contended in the Office Action, it is not clear how this teaching would further teach or suggest utilizing an immediate reset in Yamasaki.

Consequently, the proposed combination would appear to be antithetical to the fundamental principles of Yamasaki. It would require a redesign of Yamasaki in order for Yamasaki to accommodate Curiger in the manner proposed by the Examiner.

For at least these reasons, the combination of features recited in independent claims 1 and 6 when interpreted as a whole, is submitted to patentably distinguish over the prior art.

With respect to the rejected dependent claims, Appellants respectfully submit that these claims are allowable not only by virtue of their dependency from independent claim 1, but also because of additional features they recite. Examples of some of these features were discussed previously.

For all the reasons advanced above, Appellants respectfully submit that the rejection of claims 1 – 2 and 6 must be reversed.

3. The References Teach Away From the Claimed Invention.

A prior art reference must be considered in its entirety, including portions that would have lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied* 469 US 851 (1984). Where the reference teaches away from the claimed invention, it is a significant factor and must be weighed in substance. Further, known disadvantages in old devices would naturally discourage a search for new inventions, and must be taken into consideration in determining obviousness. United States v. Adams, 383 US 39, 52, 148 USPQ 479, 484 (1966).

Immediately powering off or resetting a microcomputer is undesirable for various reasons, including that immediate power off can cause random states in the microcomputer and can damage physical input/output (I/O) devices. Hence, references teach that microcomputers must provide for power off sequences.

Yamasaki discloses the conventional wisdom that immediately powering off a microcomputer is not really desirable or practical. To the contrary, the power supply is stopped only after a delay to ensure that various save operations of the computer are completed before system power off sequence is completed. Specifically, Yamasaki, col. 1, lines 20 – 29, states:

> In general, when a power switch of a computer is turned off or the voltage of the computer's built-in battery decreases, a power off signal is sent to the computer from a power supply section and power supply to the computer is inhibited after a predetermined time. Within this predetermined time, the computer stops the current job and performs a save operation to save the contents of various registers, I/O statuses, memory contents, etc., so that it can start the interrupted job when powered again.
>
> Yamasaki, col. 1, lines 20 – 29.

Yamasaki further states that stopping the power supply is problematic when the computer is accessing an input/output (I/O) device, such as a disk drive that requires a long accessing time,

where power off is likely to damage the disk drive head. (Col. 1, lines 30 – 38; see also col. 6, lines 3 – 42.)

According to U.S. Patent No. 5,721,887, Nakajima ("Nakajima"), the reset circuit resets a microcomputer when a voltage supplied to the microcomputer falls below, and remains below, a normal level for a predetermined period of time.[1] Nakajima states:

> [W]hen a time period while the source voltage is lowered is longer than the time constant, the supply of clock signals is stopped to stop the programmed operation and moreover the reset signal is generated to reset the programmed operation so that the programmed operation is executed from the initial state, when the voltage of the first power source is recovered. The program is thus prevented from being erroneously conducted. In this way, since a delay time is insured from the instantaneous cut-off of the power source to the resetting of the programmed operation, the programmed operation is never reset every time the first power source is cut off instantaneously.
>
> Nakajima, col. 2, lines 46 – 57.

Nakajima teaches away from immediately resetting a microcomputer, as the above mentioned delay is designed to avoid resetting of a programmed operation every time a first power source is cut off instantaneously.

Yamasaki and Nakajima teach that a power off or reset of a microcomputer should be delayed to prevent problems. According to Yamasaki and Nakajima, it is impractical and undesirable to have a device where "the microcomputer is reset immediately", as claimed.

Yamasaki and Nakajima are references teaching away from the claimed invention, and they are highly relevant and a significant factor to be considered in determining obviousness. The known and acknowledged problems presented by immediately resetting a microcomputer are highly relevant. It appears that these known difficulties would naturally discourage a search for a new invention where the microcomputer is reset immediately, as claimed.

[1] Nakajima was applied in the first Office Action.

Hence, the disclosures of Yamasaki and Nakajima would have led a person of ordinary skill in the art away from the invention as recited.

B. Whether claims 3 and 7 are unpatentable under 35 USC 103(a) U.S. Patent No. 5,339,446, Yamasaki et al. in view of U.S. Patent No. 6,330,668, Curiger et al. further in view of U.S. Patent No. 6,298,449, Carter.

The final office action finds independent claim 7, and claim 3 which is indirectly dependent on claim 1, to be unpatentable over Yamasaki and Curiger in view of U.S. Patent No. 6,298,449, Carter ("Carter"). According to the examiner, claims 3 and 7 are unpatentable for the reasons given in connection with claims 1, 2 and 6. The arguments above with respect to the patentability of the claimed invention over Yamasaki and Curiger are incorporated herein by reference.

The office action acknowledges that Yamasaki and Curiger do not explicitly teach detecting if any of the plurality of power sources is not set to a current in specific ranges. Carter is cited to remedy the deficiencies of Yamasaki and Curiger.

In the portions of Carter cited by the examiner as particularly relevant, Carter discloses detecting an out-of-range deviation from a power supply input voltage to a computer, time stamping data associated with the deviation and writing the data into a reliability card memory (col. 5, lines 20 – 43), and/or providing an alarm (col. 6, lines 8 – 23). The examiner also cites Carter col. 9, lines 14 – 16 as particularly relevant, discussing "a remote reboot control configured to initiate rebooting of said host computer in response to a remotely generated reboot request..."

However, Carter neither teaches nor suggests resetting the microcomputer immediately or otherwise when the supplied voltages from power sources are not within specified ranges. More

particularly, because Carter explicitly teaches that the computer takes additional action when the out-of-range deviation is detected, Carter teaches away from an immediate reset.

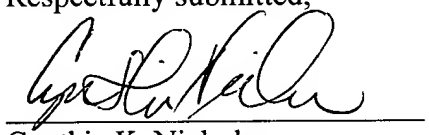
Consequently, the proposed combination would appear to be require a modification of the fundamental principles of Yamasaki and Carter, in order for Yamasaki to accommodate Curiger and Carter in the manner proposed by the Examiner.

For at least these reasons, the combination of features recited in independent claim 7 and dependent claim 3 when interpreted as a whole, is submitted to patentably distinguish over the prior art.

8. CONCLUSION

In summary, Appellants respectfully submit that claims 1 – 3 and 6 – 7 are patentable over Yamasaki, Curiger, and/or Carter, alone or in combination. Based on the comments above and in view of the evidence presented, Appellants respectfully submit that independent claims 1, 6 and 7 and dependent claims 2 – 3 are patentable under 35 U.S.C. §103(a) over Yamasaki, Curiger and/or Carter. The Examiner's rejection of claims 1 – 3 and 6 – 7 on these grounds is therefore improper and should be reversed.

Respectfully submitted,



Cynthia K. Nicholson
Reg. No. 36,880

Posz Law Group, PLC
12040 South Lakes Drive, Suite 101
Reston, VA 20191
Phone 703-707-9110
Fax 703-707-9112
Customer No. 23400

APPENDIX A – LISTING OF THE CLAIMS

1. (Previously presented) An electronic control apparatus comprising:

a plurality of power source circuits providing a plurality of power sources of a plurality of different voltages; and

a microcomputer,

wherein any one of the plurality of power sources is used as a power source of the microcomputer, and

wherein the microcomputer is reset immediately when it is detected that any one of the plurality of power sources is not set to a voltage in respective specified ranges by checking whether the plurality of power sources are respectively set to the voltages in the specified ranges.

2. (Previously presented) An electronic control apparatus as in claim 1, wherein:

the microcomputer has a CPU, a peripheral circuit, an analog-digital converting unit, a reset control unit and an oscillation circuit;

the power source circuits have a first power output circuit outputting a first voltage that is applied to the peripheral circuit and the analog-digital converting unit, and a second power output circuit outputting a second voltage that is lower than the first voltage and applied to the reset control unit, the oscillation circuit and the CPU;

a first voltage abnormality detecting circuit is provided for detecting that the first voltage is lower than a specified voltage thereof;

a second voltage abnormality detecting circuit is provided for detecting that the second voltage is lower than a specified voltage; and

the microcomputer is reset immediately when any one of the first voltage and the second voltage is detected to be lower than the first specified voltage and the second specified voltage by any one of the first and second abnormality detecting circuits.

3. (Previously presented) An electronic control apparatus as in claim 2, wherein:

a first current abnormality detecting unit is provided for detecting that a current flowing into the first power output circuit is outside a first specified range; and

a second current abnormality detecting unit is provided for detecting that a current flowing into the second power output circuit is outside a second specified range,

wherein the microcomputer is reset immediately when any one of the currents flowing into the first power output circuit and the second power output circuit is detected as being outside the first specified range and the second specified range by any one of the first current abnormality detecting circuit and the second current abnormality detecting circuit.

4. (Canceled).

5. (Canceled).

6. (Previously presented) An electronic control apparatus comprising:

a plurality of power source circuits providing a plurality of power sources of a plurality of different voltages;

a microcomputer; and

detecting means for detecting that the plurality of the power sources are set to respective specified voltages when the plurality of power sources are driven,

wherein any one of the plurality of power sources is used as the power source of the microcomputer, and

wherein the microcomputer is reset immediately when it is detected that any one of the power sources reaches the respective specified voltages.

7. (Previously presented) An electronic control apparatus comprising:

first and second power source circuits providing first and second power sources with first and second voltages different from one another, respectively;

a microcomputer connected to the first and second power source circuits and operable with the first and second voltages;

a first abnormality detection circuit for detecting an abnormal value of the first voltage and an abnormal value of a first current in the first power source circuit, the abnormal levels of the first voltage and the first current being outside predetermined first voltage and current ranges, respectively;

a second abnormality detection circuit for detecting an abnormal value of the second voltage and an abnormal value of a second current in the second power source circuit, the abnormal values of the second voltage and the second current being outside predetermined second voltage and current ranges, respectively; and

a reset control circuit for immediately resetting the microcomputer in response to an abnormality signal generated by either of the first and the second abnormality detection circuits.